Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended) A system clock divider comprising:

a divider register configured to store a mode indicator and a divisor indicator;

a divider configured to accept a first clock signal having a first frequency as an input and produce a second clock signal having a second frequency responsive thereto, said divider having a normal mode and a divide mode selectable via said mode indicator, wherein:

in said normal mode, said second frequency is substantially the same as said first frequency, ~~and~~

in said divide mode, said second frequency is ~~less~~ said first frequency divided by a divisor value corresponding to said divisor indicator; and

transition from said second frequency equal said first frequency divided by a divisor value to said second frequency substantially the same as said first frequency is synchronized to said second frequency .

Claim 2 (original) The system clock divider of claim 1, wherein said divisor value is selected from a set of divisor values including a first set of divisor values suitable for performance tuning, and a second set of divisor values suitable for power saving.

Claim 3 (currently amended) The system clock divider of claim 1, wherein said divisor value is selected from a set of divisor values, each of which ~~equal are~~ is of the form 2^n, wherein n is a whole number.

Claim 4 (original) The system clock divider of claim 1, wherein said set of divisor values is {2, 4, 8, 16, 32, 1024, 2048, 4096}.

Claim 5 (original) A system clock divider comprising:
a divider register configured to store a mode indicator and a divisor indicator;
a divider configured to accept a first clock signal having a first frequency as an input and produce a second clock signal having a second frequency responsive thereto, said divider having a normal mode and at least two divide modes selectable via said mode indicator, wherein:
in said normal mode, said second frequency is substantially the same as said first frequency,
in said first divide mode, said second frequency is less said first frequency by a divisor value corresponding to said divisor indicator; and
in said second divide mode, said second frequency is less said first frequency by a divisor value corresponding to said divisor indicator, and wherein said second divide mode is entered and/or exited through the use of a user-countable millisecond interrupt signal.

Claim 6 (original) The system clock divider of claim 5, wherein said divisor value is selected from a set of divisor values including a first set of divisor values suitable for performance tuning, and a second set of divisor values suitable for power saving.

Claim 7 (currently amended) The system clock divider of claim 5, wherein said divisor value is selected from a set of divisor values, each of which ~~equal are~~ is of the form 2^n, wherein n is a whole number.

Claim 8 (original) The system clock divider of claim 5, wherein said set of divisor values is {2, 4, 8, 16, 32, 1024, 2048, 4096}.

Claim 9 (cancelled)

Claim 10 (currently amended) A system clock divider comprising:

a register configured to store a divisor indicator;

a divider configured to accept a first clock signal having a first frequency and produce a second clock signal having a second frequency, wherein in a normal mode, said second frequency is substantially the same as said first frequency, and in a divide mode, said second frequency is less said first frequency by an amount corresponding to said divisor indicator and wherein transition from said second frequency less than said first frequency by an amount corresponding to said divisor indicator to said second frequency substantially the same as said first frequency is synchronized to said second frequency.